# We are looking for you to join our international team of successful Chip Design and Verification Engineers in our ChipGlobe Dresden/Germany Design Center.



## Senior Functional Verification Engineer (f/m/d)

ChipGlobe is focusing on Design—and Verification Consulting with both Insourcing (at Customer premises) and Outsourcing (ChipGlobe Design Center) working models. Our teams work in a global setup with ASIC design, verification and software teams in major semiconductor companies, focusing on markets in automotive, telecommunications, security and networking. ChipGlobe headquarters is located in Munich/Germany a ChipGlobe Design Center in Dresden/Germany, a ChipGlobe Design Center in Belgrade/Serbia and in Ho Chi Minh City/Vietnam as well as a ChipGlobe Entity in Singapore. We are more than 70 experts with an experienced management team. Based on the strong experience of our staff we manage and execute projects in a well-communicated, success-proven and sustainable way. We love what we do and we do what we love.

#### **ChipGlobe Offering:**

- ✓ Opportunity to work for stable, expanding German company with mature management, that is technically involved
- ✓ Excellent working environment, encouraging both technical and personal involvement
- ✓ Work together with a team of 70+ senior experts across multiple expertise domains in a global team setup
- ✓ Strategic partnerships with leading semiconductor companies. Transparent ChipGlobe yearly bonus system

#### Job requirements - Technical Skills

- √ 5+ years of experience in pre-silicon Verification based on digital and analog/mixed signal designs.
- ✓ Masters or Bachelor's degree in Electrical Engineering, Communications or an equivalent university program.
- ✓ In depth knowledge of HVL (Hardware verification Language) like SystemVerilog, 'e' and experience in building verification environments using UVM methodology.
- ✓ Domain Knowledge of Ethernet L2/L3 Switching concepts and deep understanding of Ethernet protocol is a plus.
- ✓ Functional Safety of systems/IPs ISO 26262 experience is an added advantage.
- ✓ Applying Metric driven Verification experience in projects is key.
- ✓ UPF 2.0 power aware simulations knowledge desired.
- ✓ Creating Designs using RTL (Verilog, VHDL, SystemVerilog) is a plus.
- ✓ Development of testbench concept and testbench architecture.
- ✓ Excellent design debug and root causing capabilities would be preferred.
- ✓ Knowledge of UNIX/Linux based scripting Languages like perl , python.

#### Job requirements - Soft Skills

#### ✓ Communication

- Able to abstract technical details. Open to communicate with people on and off site. Open-minded.
- Excellent communication skills, enjoys working in an international team across locations
- Very good level of spoken and written English ( at least B2 level).
- Strong presentation and listening skills are required

### ✓ Team player

- Committed to the team and task
- Helping team members, sharing knowledge

#### ✓ Self-driven and highly motivated

- Self-motivated and self-dependent worker. Embracing the task. Highlight potential issues
- Regular reporting. Clean and organized working style. Able to go the extra mile
- ✓ Solution oriented attitude, pragmatic. Good problem solving skills
  - Following and improving processes
  - Able to follow corporate reporting standards
- ✓ Organized, trusted, committed to a long term employment at Chipglobe
  - Quality awareness

If you are interested in this position, please send your CV and the reason why you would like to join ChipGlobe to: <a href="mailto:employment@chipglobe.com">employment@chipglobe.com</a>

