We are looking for you to join our international team of successful Chip Design and Verification Engineers in our ChipGlobe Munich/Germany office.

Senior DFT Engineer (f/m/d)

ChipGlobe is focusing on Design– and Verification Consulting with both Insourcing (at Customer premises) and Outsourcing (ChipGlobe Design Center) working models. Our teams work in a global setup with ASIC design, verification and software teams in major semiconductor companies, focusing on markets in automotive, telecommunications, security and networking. ChipGlobe headquarters is located in Munich, Germany with a ChipGlobe Entity in Singapore, a ChipGlobe Design Center in Belgrade, Serbia and Ho Chi Minh City, Vietnam. We are more than 70 experts with an experienced management team. Based on the strong experience of our staff we manage and execute projects in a well-communicated, success-proven and sustainable way. We love what we do and we do what we love.

You will work in a DFT Team that works on very large and challenging designs. You will work closely with RTL Engineers, Verification Engineers, and System Integration Engineers in a global setup. Besides your design related DFT verification work you will also focus on developing the DFT flow in the team that will then be used by many other groups in the company.

ChipGlobe Offering:

- ✓ Opportunity to work for stable, expanding German company with mature management, that is technically involved
- ✓ Excellent working environment, encouraging both technical and personal involvement
- ✓ Work together with a team of 70+ senior experts across multiple expertise domains in a global team setup
- ✓ Strategic partnerships with leading semiconductor companies. Transparent ChipGlobe yearly bonus system

Job requirements – Technical Skills - DFT Expert for development of MCU and MPU products, specifically

- ✓ DFT integration (implement DFT functionality in SOC/Subsystem context)
- ✓ DFT analysis with Spyglass on SOC RTL level (coverage analysis and fixes)
- ✓ DFT analysis with Mentor (Tessent) on gate level (DRC, pattern generation, coverage analysis)
- ✓ LBIST implementation, verification (RTL/Gate) and analysis
- ✓ Hierarchical scan Guidance
- ✓ DFT support for physical flow (constraints, wrapper insertion)
- ✓ Analyze scan inserted netlists with Mentor tools (coverage analysis, scan chain checks, pattern generation/re-targeting). Gate level simulation of scan pattern. Generate ATPG production pattern
- ✓ DFT verification support
- ✓ Good command of English language expected. EU working permit required.

Job requirements – Soft Skills

- ✓ **Communication**
  - Able to abstract technical details. Open to communicate with people on and off site. Open-minded.
  - Excellent communication skills, enjoys working in an international team across locations
  - Very good level of spoken and written English (at least B2 level).
  - Strong presentation and listening skills are required
- ✓ **Team player**
  - Committed to the team and task
  - Helping team members, sharing knowledge
- ✓ **Self-driven and highly motivated**
  - Self-motivated and self-dependent worker. Embracing the task. Highlight potential issues
  - Regular reporting. Clean and organized working style. Able to go the extra mile
- ✓ **Solution oriented attitude, pragmatic. Good problem solving skills**
  - Following and improving processes
  - Able to follow corporate reporting standards
- ✓ **Organized, trusted, committed to a long term employment at Chipglobe**
  - Quality awareness

If you are interested in this position, please send your CV and the reason why you would like to join ChipGlobe to:

employment@chipglobe.com